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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,703	12/21/2000	Thomas D. Nguyen	LAM1P155/P0700	9960

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EXAMINER
KORNAKOV, MICHAIL

ART UNIT	PAPER NUMBER
1746	

DATE MAILED: 08/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)
	09/747,703	NGUYEN, THOMAS D.
	Examiner	Art Unit
	Michael Kornakov	1746

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-6,9-18 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,6 and 9-18* is/are allowed.

6)☒ Claim(s) *1,4,21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 13, 2003 has been entered.

2. Claims 1, 4-6, 9-18, 21-25 are pending in the application and examined on the merits.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 4, 21-24 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation introduced in the amendment, paper No.7, namely "without performing any intervening processing steps between the etching and removal process" (col. 4, lines 60-65) is

a negative limitation that does not appear in the instant specification. Furthermore, the transitional phrase "comprising" in the instant claims with regard to the process steps, makes this limitation meaningless, since the word "comprising" permits the introduction of any process steps, including major steps. Negative limitations which do not appear in the specification as originally filed, and which introduce new concepts violate the description requirement of 35 USC 112, first paragraph, ***Ex parte Grasselli***, 231 USPQ 393 (Bd. App. 1983). This is a new matter situation.

4. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The recited limitation in claim 4 "the specific processing task is selected from etching, deposition or patterning" is indefinite, because there is absolutely no antecedent basis for such limitation in the parent claim.

5. Before the art rejection is discussed, the Examiner would like to address the issue of claim interpretation: In claim 1 the step of removing "un-wanted" particles from the backside of the wafer does not preclude or prevent cleaning of the front side of the wafer along with the back side. Therefore, as soon as the prior art describes the cleaning of back side, even along with cleaning of any other parts of the wafer, the limitation of claim 1 is met.

6. Claims 1, 4 and 25 stand rejected under 35 U.S.C. 103(a) as being unpatentable over La et al. (U.S. 6,136,510) in view of Guo et al. (U.S. 6,251,759).

La teaches a method of manufacturing a semiconductor device, which comprises the steps of providing a wafer having a front side and a backside and scrubbing the backside of the wafer **prior to performing the photolithographic** technique to remove particulate contaminants from the wafer backside (col.2, lines 10-14, lines 26-35). Backside scrubbing is effected by processing **only the backside** of the wafer by a scrubbing operation employing a brush, preferably made of a synthetic plastic, e.g. PVA. (col.4, lines 1-6) and 1% solution of NH_4OH (col.6, line 16), which is according to Applicants' definition is a semi-dry cleaning. The processing, subsequent to scrubbing the backside of the wafer, comprises etching through the photoresist mask to form a through hole, wherein plasma or reactive ion etching is utilized (col.5, lines 21-28; col.7, lines 31-37). Regarding the gaps issue, which is "maintaining desired relationship between the surface of the wafer and the chuck", La teaches that backside scrubbing removes micro defects, such as micro particles and hillocks and forms a flat plane backside surface (col.3, lines 59-64), thus eliminating gaps between the chucking surface and the backside of the wafer.

La teaches a method of manufacturing a semiconductor device, which comprises the steps of providing a wafer having a front side and a backside and scrubbing the backside (or both, see interpretation of claim 1, paragraph 6 of the instant communication) remove particulate contaminants from the wafer backside (col.2, lines

10-14, lines 26-35). Backside scrubbing is effected by processing only **th backside** of the wafer by a scrubbing operation employing a brush, preferably made of a synthetic plastic, e.g. PVA. (col.4, lines 1-6) and 1% solution of NH_4OH (col.6, line 16). The processing, subsequent to scrubbing the backside of the wafer, comprises etching through the photoresist mask to form a through hole, wherein plasma or reactive ion etching is utilized (col.5, lines 21-28; col.7, lines 31-37). Regarding the gaps issue, which is "maintaining desired relationship between the surface of the wafer and the chuck" , La teaches that backside scrubbing removes micro defects, such as micro particles and hillocks and forms a flat plane backside surface (col.3, lines 59-64), thus eliminating gaps between the chucking surface and the backside of the wafer.

While disclosing the steps of further etching or deposition on the front side of the wafer, La remains silent about **placing wafer on a chuck**, as appears in presently amended claim 1.

However, La motivates a person skilled in the art to do so by teaching that the cleaning of a backside of the wafer is employed in the process of conventional deposition and other semiconductor processing techniques. Many of these conventional techniques do include placing the wafer on the chuck for further processing. Furthermore, a chuck is a conventional element of deposition or etching apparatus, which allows to fix a wafer during processing and, therefore, a step of placing a wafer on the chuck is conventional in semiconductor processing, as evidenced, for example, by Guo (col. Fig.2; col. 5, line 66; col.6, lines 11-13). Thus, the skilled artisan would

have found it obvious to place a wafer of La on the chuck, as advised by Guo in order to properly retain the wafer during the deposition or etching procedures of La.

7. In the alternative Claims 1, 4 and 25 are separately rejected under 35 U.S.C. 103(a) as being unpatentable over La et al. (U.S. 6,136,510) in view of Loan et al. (U.S. 6,136,725).

La remains silent about the steps of placing wafer on the chuck while performing the processing task. However, as indicated above, a chuck is a conventional element of deposition or etching apparatus, which supports and keeps wafer in place during processing, therefore, a step of placing a wafer on the chuck is conventional in semiconductor processing, as evidenced, for example, by Loan (paragraph, bridging col. 8 and 9). Thus, the skilled artisan would have found it obvious to place a wafer of La on the chuck, as advised by Loan in order to properly retain the wafer during plasma or reactive ion etching procedures of La.

Allowable Claims

8. Claims 5, 6, 9-18, are allowable. The **combination** of limitations of the instant claim 5 wherein the processing sequence "consisting of" thus excluding any other steps, but recited, and wherein **only the backside of the wafer is cleaned,**
It is still the Examiner's position that La discloses strategic cleaning of only the backside ort wafer, as has been explained throughout the history of prosecution, however, La does not suggest the sequence of operations as defined in claim 5. With regard to claim

21 La does not suggest or disclose the transfer of wafer from one modulus to another with combination of action of electrostatic force and distribution of a heat transfer to the backside of the wafer.

9. Claims 21-24 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, first paragraph, set forth in this Office action.

Response to Arguments

10. Applicant's arguments filed June 11, 2003 with regard to claims 1, 4 and new claim 25 have been fully considered, but they are not persuasive. The ***crux*** of Applicants arguments appears to hinge on the preferred embodiment of La that discloses the cleaning of both sides of the wafer. Applicants further point out the difference from their claims, which call for cleaning only the backside of the wafer.

In response to this, Applicants' attention is respectfully drawn to col. 4, lines 1, and 2 wherein it is explicitly stated that "In an embodiment of the present invention backside scrubbing is effected by processing **only the backside of the wafer..." .** The recitation of La "strategically scrubbing the back side " (col. 4, lines 44, 45) also provides support for the above rejection.

Applicants address the semantics of La's statements, however, even if *arguendo, La does utilize the cleaning of both sides,* this meets the limitations set forth in claim 1, because the cleaning of a back side still takes place.

Contrary to Applicants arguments, it is still the Examiner's position that La does provide a non-preferred embodiment wherein only the back side of the wafer is cleaned

see once again col. 4, lines 1-10. What is more important, as discussed above, the construction of claims 1 and 25 does not prevent of cleaning both sides of the wafer to be processed. Resuming the above, Applicants arguments with regard to "double-side" vs. "back-side" scrubbing are much more specific than the rejected claims.

The next Applicants argument is that neither Guo, not Loan provide for the step of removing unwanted particles in order to maintain the desired relationship between the wafer and the chuck.

With regard to a Loan reference, Applicant argues that Loan does not teach sequential cleaning steps associated with wafer, and therefore, cannot be used to remedy the deficiencies of La. In response to this, it is noted, that had Loan or La taught the sequential steps, as instantly claimed, his teaching would have been used for anticipation rejection, but not as a secondary reference. The references to Loan and Guo are used to show that **placing the wafer onto the chuck is conventionally used in a semiconductor processing**. Furthermore, Loan clearly motivates a skilled artisan to utilize cleaning in a sequence with processing, by teaching that in a parallel with the main process routine other tasks can be performed (col. 13, lines 1-3).

With regard to Applicants arguments on "new matter situation" (112.1 paragraph), Applicants acknowledge that such limitation "does not appear in the Specification in its present form" however, Applicants argue that such limitation is implicit by the virtue of recitations on pages 7, 8 of Specification, as stated in paper No. 12. However, it is noted that the steps of etching, deposition or some kind of patterning

are defined by Applicants as processing steps (see page 8), and on page 15 of Specification Applicants state that the processing module can be adopted for etching, deposition, and/or the like. This statement does not prevent of performing some kind of deposition, and then patterning, and therefore, does not provide a support for the limitation "without any intervening processing steps" as per instant claims 1 and 21.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Kornakov whose telephone number is (703) 305-0400. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Randy Gulakowski can be reached on (703) 308-4333. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872 9310 for regular communications and (703) 872 9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 2450.

M. Kornakov

Michael Kornakov
Examiner
Art Unit 1746

August 8, 2003